

Amendments to the Claims

1. (*Currently Amended*) A method of reducing inter-symbol interference occurring at the digital to analog conversion of a one-bit digital signal stream, the generation of said one-bit digital signal stream (~~Se~~) ~~comprising the steps of~~ comprising the steps of:

_____ converting an input signal to said one-bit digital signal stream with a sigma-delta configuration (~~SD~~) of a low pass filter (~~F~~) having an output coupled to the input of a quantizer (~~Q~~) whose output is fed back to the input of the low pass filter,

_____ characterized by generating a control signal (~~Se~~) that is representative of the density of the edges of the one-bit digital signal stream at the output (~~θ~~) of the quantizer,

_____ multiplying the control signal (~~Se~~) with said one-bit digital signal stream (~~Se~~) and

_____ applying the result of the multiplication together with the output of the low pass filter (~~F~~) to the input of the quantizer (~~Q~~).

2. (*Currently Amended*) A one-bit sigma-delta converter for converting an input signal (~~SI~~) to a one-bit digital signal stream (~~Se~~), said converter comprising

_____ a quantizer (~~Q~~) with an input and an output,

_____ a low pass filter (~~F~~) whose output is coupled to the input of the quantizer and whose input is coupled to the output of the quantizer, thereby constituting a feedback-arrangement with the quantizer,

_____ means (~~P1~~) to supply the input signal (~~SI~~) to the feedback arrangement and

_____ means (~~θ~~) to derive the one-bit digital signal stream from the output of the quantizer, characterized by an edge-density controller (~~G~~) connected to the output (~~θ~~) of the quantizer for providing a control signal (~~Se~~) indicative of the density of the edges of the one-bit digital signal stream (~~Se~~),

_____ a multiplier (~~M~~) for multiplying said control signal (~~Se~~) with the one-bit digital signal stream (~~Se~~) of the quantizer and

_____ means (~~P2~~) for applying the output of the multiplier to the input of the quantizer.

3. (*Currently Amended*) A one-bit sigma-delta converter as claimed in claim 2 characterized in that the edge-density controller (G) comprises
_____ an edge-extractor (E) connected to receive the one-bit digital signal stream (S_e) of the quantizer, and
_____ a second low pass filter (N) receiving the output signal (SE) of the edge-extractor and providing said control signal (Se).

4. (*Currently Amended*) A one-bit sigma-delta converter as claimed in claim 3 characterized by a reference signal source (V_p) connected to the second low pass filter (N) for referencing the level of the control signal (Se).

5. (*Currently Amended*) A one-bit sigma-delta converter as claimed in claim 3 characterized in that the second low pass filter (N) is an integrator and that the reference signal is applied with a polarity opposite to that of the edge-extractor pulses to the input of the integrator.

6. (*Currently Amended*) A multi-bit sigma-delta converter for converting an input signal (S_i) to a multi-bit digital signal, said converter comprising said converter comprising:
_____ a plurality of interconnected one-bit sigma-delta converters each with a low pass filter (F) in feedback arrangement with one of a plurality (VQ) of interconnected quantizer means,
_____ means to supply the input signal to said plurality of quantizer means and means to derive the multi-bit digital signal from the outputs ($01, 02, 03$) of the plurality of quantizer means, characterized in that each of the outputs of the plurality of quantizer means is connected to an edge-density controller (G) for providing a control signal indicative of the edges of the one-bit digital stream at said output,
_____ a multiplier (M) for multiplying said control signal with the one-bit digital stream of said output and
_____ means ($P2$) for applying the result of the multiplication to the respective input of the quantizer means (VQ).

7. (*Currently Amended*) A storage medium (~~+~~) having stored thereon at least one signal track in one-bit digital stream format, characterized in that the number of clock periods comprising an edge in the one-bit digital stream of said signal track is less than 40% of the total number of clock periods of the one-bit digital stream of said signal track.